

REMARKS

Claims 1–18 are pending in the present application.

Claims 1–2 and 5–7 were amended to eliminate the unnecessary limitation of packaging the integrated circuits before mounting on the circuit board. While the exemplary embodiment of the specification packages the integrated circuits prior to mounting, such a feature is not required for successful practice of the present invention. Applicant respectfully notes that recitation of “a portion of the integrated circuit remaining exposed after packaging” is not intended to imply that the integrated circuit must be packaged at any particular point in the process, merely packaging, if occurring eventually (e.g., the product is not discarded as non-functional), should leave the identified portion of the integrated circuit exposed.

Examination of the application on the merits is respectfully requested.

**AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE**

Claims 1–2 and 5–7 were amended herein as follows:

- 1 1. (amended) A method of forming a linear photosensor array, comprising:
  - 2 forming a plurality of [packaged] integrated circuits each including a linear array of
  - 3 photosensors within [an exposed]a portion of the integrated circuit remaining exposed after
  - 4 packaging and a plurality of conductive leads adapted for soldering to a circuit board;
  - 5 mounting the [packaged] integrated circuits with the [exposed] portions containing the
  - 6 photosensors in alignment on a circuit board; and
  - 7 soldering at least some of the leads for each [packaged] integrated circuit to the circuit
  - 8 board.

1       2. (amended) The method of claim 1, wherein the step of forming a plurality of [packaged]  
2       integrated circuits each including a linear array of photosensors within [an exposed]a portion  
3       of the integrated circuit remaining exposed after packaging and a plurality of conductive leads  
4       adapted for soldering to a circuit board further comprises:

5           [for]packaging each of the plurality of integrated circuit packages by:  
6           affixing an integrated circuit die to a lead frame;  
7           connecting the integrated circuit die to selected portions of the lead frame with  
8           bond wires; and  
9           encapsulating a portion of the lead frame and the integrated circuit die except for  
10          the exposed region, wherein the exposed region of the integrated circuit die remains  
11          exposed to external ambient light.

1       5. (amended) The method of claim 1, wherein the step of forming a plurality of [packaged]  
2       integrated circuits each including a linear array of photosensors within [an exposed]a portion  
3       of the integrated circuit remaining exposed after packaging and a plurality of conductive leads  
4       adapted for soldering to a circuit board further comprises:

5           mounting a plurality of integrated circuit die on a lead frame strip with a separation  
6           between the mounted integrated circuit die approximately equal to a kerf width for a singulation  
7           saw to be used in separating the packaged integrated circuits.

1       6. (amended) The method of claim 1, wherein the step of mounting the [packaged] integrated  
2       circuits with the [exposed] portions containing the photosensors in alignment on a circuit board  
3       further comprises:

4               packaging the integrated circuits with the portion containing the photosensors exposed;  
5               and  
6       mounting adjacent packaged integrated circuits in contact with each other.

1       7. (amended) The method of claim 1, wherein the step of soldering at least some of the leads  
2       for each [packaged] integrated circuit to the circuit board further comprises:  
3               soldering only leads on one side of each [packaged] integrated circuit to the circuit board,  
4       leaving leads on an other side of the packaged integrated circuits in floating contact with  
5       conductive structures on the circuit board to facilitate adjustment and removal of [packaged]  
6       integrated circuits.

If any issue arises, or if the Examiner has any suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@novakov.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

NOVAKOV DAVIS & MUNCK, P.C.

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